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| **VELAMMAL COLLEGE OF ENGINEERING AND TECHNOLOGY, MADURAI – 625 009** |
| **Department of Computer Science and Engineering** |
| **INTERNAL ASSESSMENT - III** |

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| **Branch** | CSE | **Year/Sem./Sec.** | II/III/A,B & C |
| **Course Code** | 21EC201 | **Date** | 22-10-2024 |
| **Course Name** | Digital Principles and System Design | **Max. marks** | 50 |
| **Course Incharge** | Dr.S.Ponmalar  Mr.G.Balamuralikrishnan  Mrs.C.Swedheetha | **Time** | 01:30 Hours |

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| **PART A (Answer All Questions) (8 X 2 = 16)** | | | | |
| **Sl.No** | **QUESTION** | **K** | **CO** | **Marks** |
| 1 | Mention different modes of operation of asynchronous circuit. | K2 | CO4 | 2 |
| 2 | Define race condition. | K2 | CO4 | 2 |
| 3 | Whatis a fundamental mode asynchronous sequential circuit? | K2 | CO4 | 2 |
| 4 | What is Static-1 Hazard? | K2 | CO4 | 2 |
| 5 | What is a pulse mode asynchronous sequential circuit? | K2 | CO4 | 2 |
| 6 | Differentiate SRAM and DRAM | K2 | CO5 | 2 |
| 7 | Mention the classifications of ROM | K2 | CO5 | 2 |
| 8 | What is PROM,EEPROM & EPROM? | K2 | CO5 | 2 |

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| **PART B (Answer All Questions) (2 X 13 = 26)** | | | | |
| **Sl.No** | **QUESTION** | **K** | **CO** | **Marks** |
| 9 | Designa hazard free logic circuit for the following Boolean function. F (A, B, C, D) = ∑m (1, 3,5,7,8,9,14,15) using AND- OR gate network. (8)  (ii) Explain about Static and dynamic Hazards. (5) | K3 | CO4 | 13 |
| OR | | | | |
| 9 | What are Hazards? Explain different types of Hazard with an example. (5)  Construct a hazard free circuit for A(x, y, z) = ∑ (1, 5, 6, 7) (8) | K3 | CO4 | 13 |
| 10 | Build the circuit using PLA having 4 inputs, 6 product terms and 2 outputs F(A,B,C,D)=∑m(3,4,5,7,10,14,15), G (A, B, C, D) = ∑m (1, 5, 7, 11, 15) | K3 | CO5 | 13 |
| OR | | | | |
| 10 | Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the numbers of product terms and implement it  *A*(*x*, *y*, *z*) = ∑ (1, 3, 5, 6)  *B*(*x*, *y*, *z*) = ∑ (0, 1, 6, 7)  *C*(*x*, *y*, *z*) = ∑ (3, 5)  *D*(*x*, *y*, *z*) = ∑ (1, 2, 4, 5, 7) | K3 | CO5 | 13 |

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| **PART C (Answer All Questions) (1 X 8 = 8)** | | | | |
| **Sl.No** | **QUESTION** | **K** | **CO** | **Marks** |
| 11 | Write a behavioural VHDL description for Full Subtractor. | K3 | CO5 | 8 |
| OR | | | | |
| 11 | Write the following HDL description for 4X1 Multiplexer with Data flow/Behavioral description and Test bench. | K3 | CO5 | 8 |